VIDEO AMPLIFIER DESIGN FOR TRANSISTOR TV RECEIVERS

By Samuel A. Schwartz

I. INTRODUCTION

The primary function of the video amplifier in a television receiver is to raise the video voltage level out of the second detector to a level suitable for driving the picture tube. Certain other required outputs for auxiliary functions within the receiver are usually obtained from the video amplifier for reasons of economy and simplicity. Specifically, these are the signals necessary for driving the sound intercarrier amplifier, the sync separator, and the agc keyer stage. As a result, certain requirements are placed on the video amplifier, in addition to those necessary for driving the picture tube.

Transmission of the sound intercarrier signal through the video amplifier requires that the dynamic range of the amplifier is such that neither saturation nor collector current cutoff is attained by the maximum normal excursions of the video signal. Otherwise, uncorrectable modulation of the intercarrier signal results with a consequent noise component in the audio output. Also, a large increase in amplitude of the sound intercarrier signal by the video amplifier is desirable in order to have a minimum number of sound i-f stages.

The signals necessary for driving both the sync separator stage and the agc keyer stage must have a certain minimum level which can be best supplied by a low impedance driving source. This requirement is imposed by the characteristics of these two stages as they are both level sensitive and have a marked nonlinear input impedance.

If the video amplifier is a voltage gain stage operating directly from the second detector, it may cause severe bandwidth limiting of the second detector output due to its large Miller capacitance. Lower collector-to-base capacitance of future video transistors that may be developed will probably not reduce the bandwidth limiting to an acceptable degree. Considering a collector-to-base capacitance, including external strays, of only two (2) picofarads and a stage gain of 40 with the rather low value of detector load resistance of 2 kilohms, the second detector uncompensated bandwidth would be only 1 mc. This situation could be improved by reducing the second detector load resistance, but other objectionable effects would occur. The output power required from the second detector would have to be increased thereby placing higher power demand on the i-f amplifier. The higher level at the second detector also would complicate the detector shielding associated with preventing i-f harmonic radiation back into the receiver front end.

The video amplifier configuration that satisfies these requirements consists of a common-collector stage driving a common-emitter stage which are termed the video driver and video output, respectively. The driver is d-c coupled to the second detector circuit and is a-c coupled to the output stage. This type of circuit was used in the experimental receiver that was built and it will be used as an example in the following discussion.

A second detector output level of 3 V p-p with a positive going sync polarity results in the proper amplitude of signal at the output of the video driver

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stage for driving a sync separator employing an NPN transistor. The low output impedance from the video driver prevents sync compression which could be caused by the low input impedance of the sync separator during the synchronizing interval. The use of d-c coupling between the second detector and the driver results in a driver output that has an absolute sync level with respect to ground. This signal is thus suitable for driving the agc keyer stage. The bias on the video driver stage should be set so that the transconductance from base to collector is essentially linear over the video signal range of 3 volts, thereby passing the sound intercarrier signal with unobjectionably small distortion. This bias is such that the video signal at the emitter of the video driver swings between the level of +2 volts at zero detected signal up to a maximum of +5 volts on sync tips. The lower limit is set by the bias network for the stage, while the upper limit is controlled by the agc system which is actuated by the +5 volt level. By placing a 4.5 mc transformer in the collector circuit of the video driver, the stage becomes a narrow-band common-emitter bandpass amplifier centered at 4.5 mc. A 4.5 mc series trap placed from the emitter to ground reduces the degeneration and thus raises the voltage gain at 4.5 mc.

II. DESIGN OF VIDEO OUTPUT STAGE

The required bandwidth from the second detector to the video output is 3.2 to 4 mc depending upon the quality of the receiver. The 4 mc figure will be used in this design in order to demonstrate device capability. As was previously discussed, a common collector stage greatly reduces the capacitive loading of the second detector. Thus, it is possible to achieve a second detector bandwidth greater than 4 mc while allowing the video output stage to have a bandwidth of 4 mc. This expedient reduces the bandwidth shrinking normally present in cascaded stages having identical bandwidths.

Since the required bandwidth of 4 mc is very close to f_β of the Fairchild S5310E video output transistor, conventional shunt, series, or shunt-series peaking can be used to afford a bandwidth improvement over the conventional RC bandwidth limited stage.[1] The shunt peaking arrangement was chosen over the other alternatives for the following reasons: Since the S5310E planar transistor permits a high power dissipation a comparatively small collector load resistor is allowable resulting in an RC limited bandwidth greater than 2 mc in the collector circuit. A bandwidth improvement by a factor of 1.8 can be obtained by shunt peaking with a corresponding pulse response overshoot of only 5 per cent (Ref. 2). Further, series and shunt-series peaking schemes require a definite capacitance ratio between each end of the load network for best performance; whereas the shunt peaked scheme utilizes the total lumped capacitance. Shunt peaking requires fewer components and less circuit accuracy, thus it was used to obtain the necessary bandwidth.

Using the shunt peaked scheme, the bandwidth improvement factor is 1.8. Therefore, the required RC bandwidth, β_μ, is as follows:

$$\beta_\mu = 4 \text{ mc}/1.8 = 2.22 \text{ mc}$$

Note that this value is limited only by the passive component networks and not by the active device. Bandwidth limiting due to the transistor is given in Appendix Eq. 8A.

The required collector load resistor, R_L, with a total shunt capacitance C_T is

$$R_L = \frac{1}{2\pi\beta_\mu C_T}$$

$$= \frac{1}{2\pi(2.22 \times 10^6)\,(25 \times 10^{-12})}$$

$$= 2.86 \text{ K} \qquad (1)$$

where

$$C_T = C_{oe} + C_{gi} + C_s$$

$$= 15 + 5 + 5 = 25 \text{ pf}$$

Using a standard value for R_L = 3 KΩ compute the peaking coil size L_C as follows:

$$L_C = m(R_L)^2 C'_T \qquad (2)$$

Letting m = 0.46 for 5 per cent overshoot

$$L_C = 0.46(3 \times 10^3)^2 \times (25 \times 10^{-12})$$
$$= 103.5\ \mu h$$

The video drive requirement for conventional picture tubes is approximately 110 volts p-p video for cathode drive while an additional 10 per cent of drive voltage is required for grid drive. In order to satisfy the auxiliary takeoff requirements, the video polarity at the output of the video amplifier is such that sync and blanking go negative, therefore grid drive of the picture tube is necessary. Thus, the video amplifier must supply a video signal having 120 volts p-p for driving the picture tube grid. The S5310E video amplifier transistor is a silicon planar device having an LV_{CEO} rating of 150 volts. A choice of collector supply voltage of 140 volts allows a collector swing of 120 volts with an adequate voltage margin at each end of the range.

Refer to Fig. 1 for the collector load line construction on the collector characteristics.

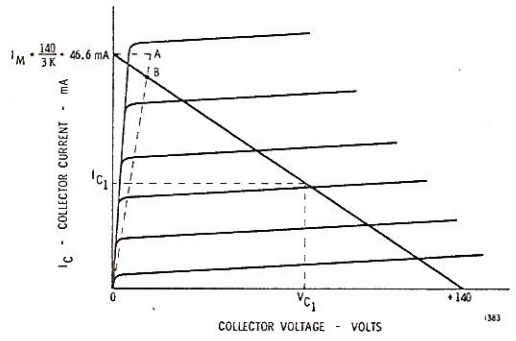

FIG. 1. Construction of load lines.

This graphical construction adequately defines large signal operation and is thus useful for high-level output stages. The locus of the resistive load line represents collector voltages at various base drive conditions. A second line OA defines the lower limit of collector swing as determined by the voltage drop across the emitter resistor and the collector-to-emitter saturation voltage. In order to construct OA it is first necessary to determine the value of the emitter resistor.

Assuming a voltage source driving the video amplifier and r'_e which is small due to appreciable emitter current, the value R_E can be calculated as follows:

$$R_E \approx R_L/A_V \qquad (3)$$

when R_L = 3 K ohms and A_V = 48

$$R_E \approx 3000/48 = 62.5\ \Omega$$

It is necessary to define point A at a value of collector current no higher than V_{CC}/R_L. Therefore, the voltage at point A is

$$V_A = V_{CE}(sat) + \frac{V_{CC}}{R_L} R_E \qquad (4)$$

If it is assumed that the collector saturation characteristic is essentially linear from the origin to point A, a straight line can be drawn from O to A. The intersection of line OA with the load line at point B represents the lower limit of collector swing and typically is

$$V_B \approx V_A = V_{CE}(sat) + \frac{V_{CC}}{R_L} R_E \qquad (5)$$

$$= 0.5 + \frac{140}{3 \times 10^3}(62.5) = 3.4 \text{ volts}$$

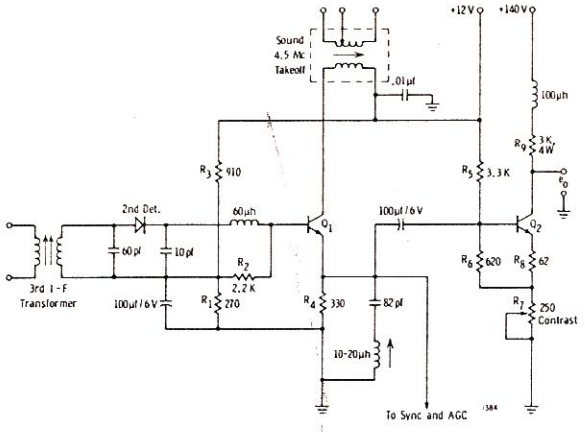

FIG. 2. Schematic diagram of video amplifier.

The video signal is a-c coupled into the video output stage for reasons of bias stability as shown in Fig. 2. However, there are certain advantages to be gained in the presence of high impulse noise by d-c coupling the video output stage to the video driver, but more elaborate coupling networks are required. Using the a-c coupled configuration, the quiescent bias point can be established by assuming that the average video signal will have equal positive and negative peaks for an a-c coupled or area balanced waveform. Thus the bias point can be chosen as follows:

$$I_{C_1} = (V_{CC} - V_B)/2R_L$$
$$= (140 - 3.4)/2 \times 3 \times 10^3$$
$$= 22.8 \text{ mA} \qquad (6)$$

The corresponding collector voltage V_{C_1}, then, is given by

$$V_{C_1} = V_{CC} - I_{C_1} R_L$$
$$= 140 - (22.8 \times 10^{-3})(3 \times 10^{-3})$$
$$= 71.7 \text{ volts} \qquad (7)$$

This bias point represents the condition of maximum transistor dissipation (Ref. 3), therefore it is necessary to ascertain whether or not device capability is exceeded.

$$P_{diss} = I_{C_1} V_{C_1}$$
$$= (22.8 \times 10^{-3})(71.7)$$
$$= 1.64 \text{ watts} \qquad (8)$$

This dissipation is close to the 100°C case temperature rating of 1.7 watts for the device. Therefore for operation in ambients up to 71°C, a radiator should be placed on the transistor whose thermal resistance is not greater than

$$R_T = \frac{100° - 71°}{1.7} = 17°\text{C/Watt} \qquad (9)$$

The use of a finned radiator having a thermal resistance of 15° C/watt proved to be adequate.

Video contrast is controlled by gain adjustment of the video output stage. By increasing the resistance in the emitter circuit over the minimum value required for maximum gain setting, the stage gain is reduced. The maximum value of emitter resistance should allow the gain to vary over a range of approximately 4 to 1. Over this range of control, the stage bias should remain essentially constant to prevent large changes in the quiescent collector voltage that could cause compression of the video output signal. Proper bias is established by connecting the base biasing network consisting of resistors R_5 and R_6 to the junction of the fixed and variable emitter resistances R_7 and R_8 respectively. The values of the resistors are determined by conventional biasing techniques for providing adequate d-c stability as well as controlling the quiescent collector current.

The video driver, that provides the video voltage source for several loads, obtains a low output impedance by means of its common collector configuration. The emitter resistor and the base biasing resistors R_4, R_1, R_2, and R_3, respectively, are designed to provide a +2 volt output level in the absence of an input video signal.

The corresponding emitter current of 6 mA allows the full input signal excursion to transverse the broad peak of the β vs. I_C curve for the SE1001 transistor used in the video driver.

The voltage drop across resistor R_2 due to the d-c component of base current for the video driver transistor Q_1, serves to forward bias the second detector diode and thus aid in making the detector characteristic linear.

The bandwidth of the video driver is limited by the output resistance of the stage in combination with the input capacitance of the video output stage. Considering the detector output impedance equal to the detector load resistance, the output resistance R_O is found from the expression

$$R_O \approx \frac{R_E \left[R_g / (\beta_0 + 1) \right]}{R_E + R_g / (\beta_0 + 1)} \approx \frac{330 \left[2200/(40+1) \right]}{330 + 2200/(40+1)}$$

$$\approx 46.2\ \Omega \qquad (10)$$

The input capacitance, C_{in}, of the video output stage is primarily Miller capacitance, and it is calculated as follows:

$$C_{in} = C_s + C_{ob}(A + 1)$$
$$= 6 + 5(48 + 1)$$
$$= 251\ \text{pf} \qquad (11)$$

The RC limited bandwidth β_μ is shown below:

$$\beta_\mu = 1/(2\pi R_O C_{in})$$
$$= 1/[2\pi(46.2)(251 \times 10^{-12})]$$
$$= 13.8\ \text{mc} \qquad (12)$$

As the second detector bandwidth is considerably higher than that of the video amplifier; no bandwidth compensation was applied to the circuit.

III. CONCLUSION

It has been shown that the overall requirements for a television receiver video amplifier are satisfied by the common collector stage driving a common emitter feedback stage. The basic bandwidth limiting mechanisms are the associated load networks for the stages while the transistors operating with degenerative feedback produce only a minor effect. Silicon planar transistors having high dissipation, high LV_{CEO} ratings, and high f_t ratings make possible high output voltages with simple conservatively designed circuits having high reliability.

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APPENDIX

I VOLTAGE GAIN EQUATIONS

Using the approximate equivalent circuit of the video transistor, the overall equivalent circuit of the video amplifier is shown in Fig. 1A. The collector-base capacitance C_C is shown as a Miller capacitance shunting the emitter diffusion capacitance. The input impedance, h'_{ie}, to the amplifier at terminals b – g is given in the expression

$$h'_{ie} = r'_b + \frac{R}{1 + s C_T R} + R_E (h_{fe} + 1)$$

where

$$C_T = 1/(\omega_\beta R) + C_C (A + 1)$$
$$= [1 + \omega_\beta R C_C (A + 1)] / (\omega_\beta R)$$
$$h_{fe} = (\omega_\beta \beta_0)/(\omega_\beta + s)$$
$$s = j\omega$$

so that the equation for h'_{ie} becomes

$$h'_{ie} = r'_b + \frac{R}{1 + sR\left[\frac{1 + \omega_\beta R C_C (A + 1)}{\omega_\beta R}\right]} + R_E \left(\frac{\omega_\beta \beta_0}{\omega_\beta + s} + 1\right)$$

$$= r'_b + R_E + \frac{\omega_\beta \beta_0 R_E}{\omega_\beta + s} + \frac{\omega_\beta R}{\omega_\beta + s [1 + \omega_\beta R C_C (A + 1)]} \quad (1A)$$

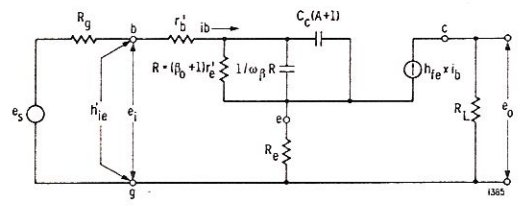

FIG. 1A. Equivalent circuit of emitter-feedback stage.

The gain of the amplifier can be expressed as follows:

$$A_V = e_o / e_i$$
$$= -(h_{fe} i_b R_L) / (i_b h'_{ie}) = -(h_{fe} R_L) / h'_{ie}$$

Substituting the equations for h'_{ie} and h_{fe} in the above and simplifying yields the following:

$$A_V = -(\omega_\beta \beta_0 R_L) \Bigg/ \Bigg\{ \omega_\beta [R_E (\beta_0 + 1) + r'_b] + s (R_E + r'_b) + \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s [1 + \omega_\beta R C_C (A_V + 1)]} \Bigg\} \quad (2A)$$

The third term in the denominator still contains an A_V term. The final solution for A_V involves a lengthy quadratic equation that does not serve a practical purpose. The equation can be simplified by taking the limit as s approaches 0.

$$\lim_{s \to 0} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s [1 + \omega_\beta R C_C (A_V + 1)]} = \omega_\beta R$$

Thus the expression for low frequency gain becomes

$$A_{V_0} = -\frac{\omega_\beta \beta_0 R_L}{\omega_\beta [R_E (\beta_0 + 1) + r'_b] + \omega_\beta R}$$

$$= -\frac{\beta_0 R_L}{R_E (\beta_0 + 1) + r'_b + R}$$

Substituting

$$R = (\beta_0 + 1) r'_e$$

$$A_{V_0} = \frac{\beta_0 R_L}{R_E (\beta_0 + 1) + r'_b + (\beta_0 + 1) r'_e}$$

$$= -\frac{\beta_0 R_L}{(R_E + r'_e)(\beta_0 + 1) + r'_b} \quad (3A)$$

Since $(R_E + r'_e)(\beta_0 + 1) \gg r'_b$ and $(\beta_0 + 1) \simeq \beta_0$ then

$$A_{V_0} \simeq - \frac{R_L}{R_E + r'_e}$$

$$\simeq - \frac{R_L}{R_E + 26/I_E} \qquad (4A)$$

For the practical video amplifier supplying a high output voltage, the emitter current must be correspondingly high, therefore $r'_e = 26/I_E$ will be small compared to R_E. A further simplification results for A_{V_0}.

$$A_{V_0} \simeq - \frac{R_L}{R_E} \qquad (5A)$$

The effect of the third term in the denominator, Eq. (2A), on the overall gain function is as follows: as $s \to \infty$ the resulting indeterminate form may be bypassed and a determinate form obtained by noting that the

$$\lim_{s \to \infty} \frac{f(s)}{F(s)} = \lim_{s \to \infty} \frac{f'(s)}{F'(s)}$$

$$\lim_{s \to \infty} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s [1 + \omega_\beta R C_C (A_V + 1)]}$$

$$= \frac{R \omega_\beta}{1 + \omega_\beta R C_C (A_V + 1)}$$

The denominator of the limit can be evaluated for a typical video amplifier transistor using the following values:

$$\omega_\beta = \frac{2\pi \times 150 \times 10^6}{\beta_0 + 1} \; ; \; R = (\beta_0 + 1) \; ; \; C_C = 10 \text{ pf} \; ;$$

$$A_V = 15$$

$$\text{Denominator} = 1 + \left[\frac{2\pi (150 \times 10^6)}{\beta_0 + 1}\right] \left[\beta_0 + 1\right] \left[10^{-11}\right]$$

$$\cdot \left[15 + 1\right] = 1.15$$

The practical limit for the third term in the denominator of the gain function, Eq. (2A), using typical transistor values is

$$\lim_{s \to \infty} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s [1 + \omega_\beta R C_C (A_V + 1)]} = \frac{R \omega_\beta}{1.15}$$

$$\frac{R \omega_\beta}{1.15} = \frac{(\beta_0 + 1) r'_e \omega_\beta}{1.15}$$

By combining the above term, lim D_3, with the first term, D_1, in the denominator of A_V, Eq. (2A), is

$$D_1 + \lim D_3 = \omega_\beta [R_E (\beta_0 + 1) + r'_b] + \frac{\omega_\beta (\beta_0 + 1) r'_e}{1.15}$$

$$= \omega_\beta \left[\left(R_E + \frac{r'_e}{1.15} \right) (\beta_0 + 1) + r'_b \right]$$

It can be seen that where $R_E \gg r'_e/1.15$, the effect of Miller capacitance has a minimal effect on the denominator of the gain function, therefore, the equation for the gain function becomes

$$A_V = - \frac{\omega_\beta \beta_0 R_L}{\omega_\beta [R_E (\beta_0 + 1) + r'_b] + s (R_E + r'_b)} \qquad (6.1A)$$

From Eq. (6.1A), the pole of the gain function is located at (see Fig. 2A)

$$s = - \frac{1}{R C'_{be}} \left[\frac{R_E (\beta_0 + 1) + r'_b}{R_E + r'_b} \right]$$

If the gain function in Eq. (6A) is modified to include the capacitance C'_T normally present in the actual circuit shunting the collector load resistance, R_L, the following results:

$$A_V = - \frac{\omega_\beta \beta_0 R_L}{(1 + s C'_T R_L)\{\omega_\beta [R_E(\beta_0 + 1) + r'_b] + s(R_E + r'_b)\}} \qquad (6.2A)$$

From Eq. (6.2A), the poles of the gain function are located at (see Fig. 3A)

$$s = - \left[\frac{1}{R C'_{be}}\right] \left[\frac{R_E(\beta_0 + 1) + r'_b}{R_E + r'_b}\right]; \quad s = - \frac{1}{R_L C'_T}$$

The use of a shunt peaking coil, L_C, for bandwidth compensation modifies the gain function to the following equation:

$$A_V = - \frac{\omega_\beta \beta_0 (R_L + s L_C)}{(s^2 L_C C'_T + s R_L C'_T + 1)\{\omega_\beta [R_E(\beta_0 + 1) + r'_b] + s(R_E + r'_b)\}} \qquad (6.3A)$$

The value of the peaking coil is dependent on the rise time improvement or bandwidth compensation desired consistent with the permissible overshoot and is expressed in terms of a parameter m such that

$$L_C = m R_L^2 C'_T \qquad (6.4A)$$

Substitution of Eq. (6.4A) in Eq. (6.3A) yields the following:

$$A_V = - \frac{\omega_\beta \beta_0 (R_L + s m R_L^2 C'_T)}{(s^2 m R_L^2 C'^2_T + s R_L C'_T + 1)\{\omega_\beta [R_E(\beta_0 + 1) + r'_b] + s(R_E + r'_b)\}} \qquad (6.5A)$$

From Eq. (6.5A) the poles of the gain function are located at (see Figs. 4A and 5A)

$$s = - \frac{1}{R C'_{be}} \left[\frac{R_E(\beta_0 + 1) + r'_b}{R_E + r'_b}\right]$$

$$s = \frac{1}{R_L C'_T} \left(\frac{1}{2m}\right)(-1 \pm j\sqrt{4m - 1})$$

From Eq. (6.5A) the zero of the gain function is located at (see Figs. 4A and 5A)

$$s = - \frac{1}{m R_L C'_T}$$

From the complex frequency plot of Eq. (6.1A) it is shown that the bandwidth is very wide for the amplifier gain function where the value of R_E is significantly large. The plot also represents the amplifier transadmittance so that the emitter circuit response of the amplifier is simultaneously defined (approximately). Thus, in Eq. (10) where output resistance is defined in terms of β_0 rather than h_{fe}, the simplified equation is valid.

The effect of shunt capacitance across the collector load resistance introduces a second pole on the σ axis. This causes the bandwidth of the practical video amplifier to be significantly reduced over that obtained with the emitter degene-

rated transistor with a pure resistive load.

The use of shunt peaking allows a bandwidth improvement over that obtained by the $R_L C'_T$ limited case in Eq. 6.2A. As the parameter m, and thus the value of the peaking inductance, is increased from zero, a single real pole starts from $-1/(R_L C'_T)$ and moves toward $-2/(R_L C'_T)$ while a second real pole moves from $-\infty$ and coincides with the first real pole at $-2/(R_L C'_T)$ when m = 0.25. As m is increased further, both poles become complex and follow a circular path approaching the origin at m = ∞ as shown in Fig. 5A. For values of m up to 0.25, the resulting time response contains no overshoot, because the poles remain on the real axis and can contribute only to neper frequencies rather than radian frequencies. As m is increased beyond 0.25 the time response will contain overshoot due to the radian frequency enhancement by the resulting complex poles. A practical value for m = 0.46 is satisfactory for television video amplifiers where the time response is only 5% for a bandwidth improvement factor of 1.8.

Bandwidth limiting in the amplifier due to the frequency-sensitive elements within the transistor and excluding the effect of the collector-circuit time constant existing in the practical circuit can be expressed by Eq. (7A) below. The generator resistance, R_s, is included although the Miller

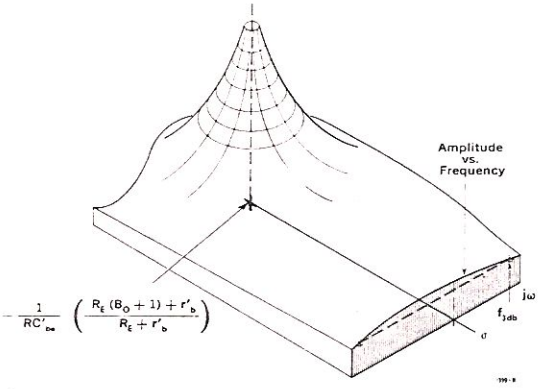

FIG. 2A. Complex frequency plot of amplifier gain function with resistive load (Eq. 6.1A).

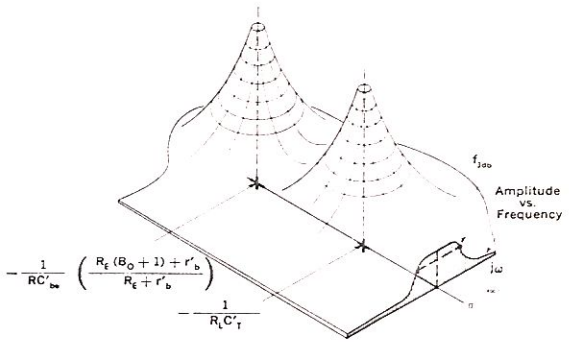

FIG. 3A. Complex frequency plot of amplifier gain function with resistive load shunted by circuit capacitance (Eq. 6.2A).

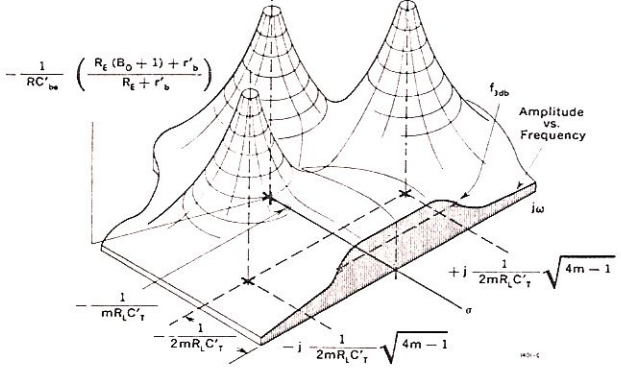

FIG. 4A. Complex frequency plot of amplifier gain function with load consisting of R_L, C'_T, and L_C (Eq. 6.3A)

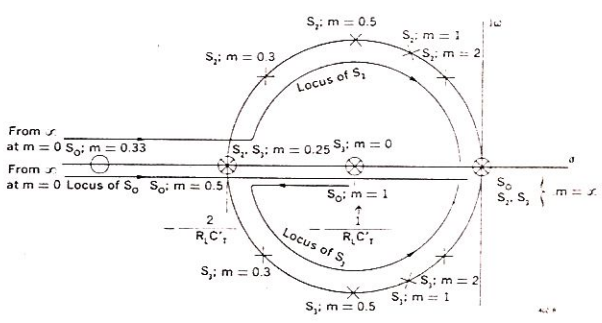

FIG. 5A. Pole-zero locus plot as a function of parameter *m*.

effect capacitance is excluded based on the foregoing description.

$$\frac{e_o}{e_s} = -\frac{h_{fe} R_L}{R_S + h'_{ie}}$$

$$= -\left(\frac{\omega_\beta \beta_0}{\omega_\beta + s}\right) R_L \Bigg/ \left\{ R_S + r'_b + \frac{R}{1 + s R[(1/\omega_\beta R)]} + R_E \left[\frac{\omega_\beta \beta_0}{\omega_\beta + s} + 1\right]\right\}$$

$$= -(\omega_\beta \beta_0 R_L) \Big/ \{\omega_\beta [R_S + r'_b + R + R_E(\beta_0 + 1)] + s(R_S + r'_b + R_E)\} \quad (7A)$$

The 3 db bandwidth occurs at a frequency where the real and imaginary parts of the denominator are equal, which is

$$|\omega_\beta [R_S + r'_b + R + R_E(\beta_0 + 1)]| = |s(R_S + r'_b + R_E)|$$

$$\omega_\beta [R_S + r'_b + R + R_E(\beta_0 + 1)] = \omega_{3db}(R_S + r'_b + R_E)$$

$$\omega_{3db} = \frac{\omega_\beta [R_S + r'_b + R + R_E(\beta_0 + 1)]}{R_S + r'_b + R_E}$$

$$f_{3db} = \frac{\frac{f_t}{\beta_0 + 1}[R_S + r'_b + r'_e(\beta_0 + 1) + R_E(\beta_0 + 1)]}{R_S + r'_b + R_E}$$

$$= \frac{f_t\left[R_E + r'_e + \frac{R_S + r'_b}{\beta_0 + 1}\right]}{R_S + r'_b + R_E} \quad (8A)$$

The typical video amplifier transistor and video driver exhibit the following values:

$r'_b = 10\ \Omega$ $\quad R_S = 50\ \Omega$
$r'_e = 1\ \Omega$ 26 mA $\quad \beta_0 = 50\ \Omega$
$R_E = 62\ \Omega$ $\quad f_t = 150$ Mc

$$f_{3db} = \frac{150 \times 10^6 \left[62 + 1 + \frac{50 + 10}{50 + 1}\right]}{50 + 10 + 62} = 79 \text{ Mc}$$

Thus it may be seen that the transistor with emitter feedback has little effect on the frequency response within the 4 mc band of interest.

II. ANALYSIS OF COMMON COLLECTOR VIDEO DRIVER

The equivalent circuit of the video driver is shown in Fig. 6A. Collector capacitance C_C will not be taken into account since its effect is much less in the common collector stage than in the emitter feedback amplifier where it was inconsequential.

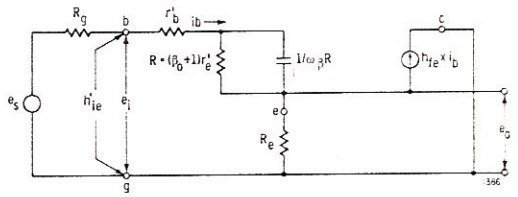

FIG. 6A. Equivalent circuit of common-collector stage.

The input impedance h'_{ie} at terminals $b - g$ is given in the expression below.

$$h'_{ie} = r'_b + \frac{R}{1 + s C'_{be} R} + R_e(h_{fe} + 1)$$

$$= r'_b + R_E + \frac{R}{1 + \frac{s}{\omega_\beta}} + R_E\left(\frac{\omega_\beta \beta_0}{\omega_\beta + s}\right)$$

$$h'_{ie} = r'_b + R_E + \frac{R\omega_\beta}{\omega_\beta + s} + \frac{R_E \omega_\beta \beta_0}{\omega_\beta + s} \quad (9A)$$

The gain of the video driver can be expressed as follows:

$$A_V = \frac{e_o}{e_i}$$

$$= \frac{R_E (h_{fe} i_b + i_b)}{i_b (h'_{ie})}$$

$$= \frac{R_E (h_{fe} + 1)}{h'_{ie}}$$

$$= \frac{R_E \left[\frac{\omega_\beta \beta_0}{\omega_\beta + s} + 1 \right]}{r'_b + R_E + \frac{R \omega_\beta}{\omega_\beta + s} + \frac{R_E \omega_\beta \beta_0}{\omega_\beta + s}} \qquad (10A)$$

The expression for low frequency gain A_{V_0} is

$$A_{V_0} = \frac{R_E [\omega_\beta (\beta_0 + 1)]}{\omega_\beta [R_E (\beta_0 + 1) + R + r'_b]}$$

$$= \frac{R_E (\beta_0 + 1)}{R_E (\beta_0 + 1) + R + r'_b} \qquad (11A)$$

In order to derive the bandwidth of the video driver it is necessary to include the effect of its driving source resistance in the voltage gain equation.

$$\frac{e_o}{e_s} = \frac{R_E (h_{fe} i_b + i_b)}{i_b (h'_{ie} + R_S)}$$

$$= \frac{R_E (h_{fe} + 1)}{h'_{ie} + R_S}$$

$$= \frac{R_E \left[\frac{\omega_\beta \beta_0}{\omega_\beta + s} + 1 \right]}{r'_b + R_E + \frac{R \omega_\beta}{\omega_\beta + s} + \frac{R_E \omega_\beta \beta_0}{\omega_\beta + s} + R_S}$$

$$= \frac{R_E [\omega_\beta (\beta_0 + 1) + s]}{\omega_\beta [R_E (\beta_0 + 1) + R_S + R + r'_b] + s (R_E + R_S + r'_b)}$$

The 3 db bandwidth occurs at a frequency where the real and imaginary parts of the e_o/e_s denominator are equal

$$| \omega_\beta [R_E (\beta_0 + 1) + R_S + R + r'_b] | = | s (R_E + R_S + r'_b) |$$

$$\omega_\beta [R_E (\beta_0 + 1) + R_S + R + r'_b] = \omega_{3db} (R_E + R_S + r'_b)$$

$$\omega_{3db} = \frac{\omega_\beta [R_E (\beta_0 + 1) + R_S + R + r'_b]}{R_E + R_S + r'_b}$$

$$f_{3db} = \frac{\frac{f_t}{\beta_0 + 1} [R_E (\beta_0 + 1) + R_S + r'_e (\beta_0 + 1) + r'_b]}{R_E + R_S + r'_b}$$

$$= f_t \frac{\left[R_E + r'_e + \frac{R_S + r'_b}{\beta_0 + 1} \right]}{R_E + R_S + r'_b} \qquad (12A)$$

Typical values for the video driver circuit and the detector source resistance can now be substituted into Eq. (12A); these are: $R_E = 300\,\Omega$, $R_S = 2200\,\Omega$, $r'_e = 26/10$ mA $= 2.6\,\Omega$, $\beta_0 = 50$, $r'_b = 15\,\Omega$, and $f_t = 250 \times 10^6$.

Solving for bandwidth

$$f_{3db} = \frac{250 \times 10^6 \left[300 + 2.6 + \frac{2200 + 15}{50 + 1} \right]}{300 + 2200 + 15}$$

$$= 34.4 \text{ Mc}$$

Thus it can be seen that even with the large value of detector source resistance, the frequency response of the video driver has a small effect on the 4 mc video passband.

LIST OF SYMBOLS

A_V	Voltage gain of stage
A_{Vo}	Low frequency or d-c voltage gain
C'_{be}	Emitter diffusion capacitance
C_C	Collector-to-base capacitance (approximately equal to C_{ob})
C_{gi}	CRT grid input capacitance
C_{in}	Input capacitance of the video output stage
C_{oe}	Output capacitance, common-emitter
C_S	Stray capacitance
C_T	Sum of emitter-diffusion capacitance and Miller capacitance
C'_T	Total shunt capacitance
f_{3db}	Cutoff frequency of the amplifier
f_T	Gain bandwidth product
h_{ie}	Input impedance of the amplifier at terminals b-g
I_{C1}	Collector current at the quiescent bias point
L_C	Peaking coil inductance in collector circuit
m	Parameter of peaking coil inductance
P_{diss}	Power dissipation in the output transistor
r'_b	Intrinsic base resistance
r'_e	Intrinsic emitter resistance
R_E	Emitter resistor
R_o	Output resistance of video driver
R_L	Video load resistance
R_S	Resistance of the source
R_T	Thermal Resistance
s	Complex variable
V_A	Voltage at point A on load line of the graphical construction
V_B	Voltage at point B on load line of the graphical construction
V_{C1}	Collector voltage at the quiescent bias point
V_{CC}	Collector supply voltage
$V_{CE}(sat)$	Collector-to-emitter saturation voltage
β_o	Low frequency transistor forward current transfer ratio
β_μ	Uncompensated bandwidth
ω_β	Radian cutoff frequency of β
ω_{3db}	Radian cutoff frequency of the amplifier